**Prism Memory – Flash ROM**

Prism’s ROM is provided by a flash chip. When not in ‘safe’ mode, ‘flash programming’ mode or a +2A/+3 ‘all memory’ mode, the first 16K of Prism’s memory is the flash chip (in read-only mode) acting as ROM, just like on a Spectrum.

The flash chip is split into 256 lots of 16K. Which of these 256 flash pages is paged in is controlled by a register at IO address **0xEE3B (60987)**.

The least significant bit (bit 0) of this register is also changed by **bit 4** of IO port **0x7FFD (32765)**, which means that 32K ROMS (eg the 128K Spectrum ROM and SE BASIC IV) work as expected when split into 16K chunks, so long as the pair of 16K ROM images are loaded with ‘ROM0’ of the pair flashed to an even numbered flash page and ‘ROM1’ flashed to the following page.

The second least significant bit (bit 1) of this register is also changed by **bit 2** of IO port **0x1FFD (8189)** which means that 64K ROMS (eg the +3 ROM or +3e ROMs) will work as expected when split into 16K chunks so long as ‘ROM0’ of the four 16K ROM images is flashed to a flash page which is a multiple of ‘4’ (so flash page 0,4,8,12,16 etc etc), ROM1 is flashed to the following page, ROM2 is flashed to the next etc.

It is recommended that, where available to you, the following ROM images be flashed to the following pages (that way it matches the development Prism):

0 – Prism boot ROM 0\* (This is the default ROM paged in at power-up)

1 – Prism boot ROM 1\*

2 – Spectrum 48K ROM

3 – Spectrum 48K ROM (with the divMMC automapper enabled)

4 – SE BASIC IV ROM0

5 – SE BASIC IV ROM1

6 – SE BASIC IV ROM0

7 – SE BASIC IV ROM1

8 – Spectrum 128 ROM0

9 – Spectrum 128 ROM1

10 – Spectrum 128 ROM0

11 – Spectrum 128 ROM1

16 – Spectrum +3eMMC ROM0

17 – Spectrum +3eMMC ROM0

18 – Spectrum +3eMMC ROM0

19 – Spectrum +3eMMC ROM0

64 – esxDOS (this is an 8K ROM, so it is repeated twice in this flash page)

65 – Multiface 128 (this is an 8K ROM, so it is repeated twice in this flash page)

*\* currently, the development Prism has the Spectrum 48K ROM in flash pages 0 and 1 too as the BOOT ROM is still in development*

**Safe Mode**

Safe Mode is activated by pressing the ‘f9’ key. When it is activated, a known-good ROM image is paged into the first 16K of Prism’s memory. This ROM image is hard-coded within Prism’s FPGA and is not stored on the flash chip.

Safe mode is used when you first power-up Prism for the first time and you need to flash ROM images to Prism’s flash chip. It also lets you recover from flash chip corruption or accidental deletion should that occur.

Once activated, Safe Mode can only be deactivated by a hard reset (f12) or power cycle.

*\* currently the ‘safe mode’ ROM in the development Prism is the 48K Spectrum ROM image. As this ROM cannot be legally distributed with new hardware, this will later be replaced with the Prism BOOT ROM0.*

**Flash Programming Mode**

Programming mode reconfigures Prism so that the flash can be programmed. When activated, the safe mode ROM is paged into the first 16K of Prism’s memory and the currently selected flash page is paged into RAM at 0x8000 (32768) and write access to the flash chip is enabled.

To activate programming mode, you must set one of the ULA2 4-bit registers (register 15) at IO 0x8E3B (36411) to a specific value (1010 binary):

OUT 36411, 250 – enters flash programming mode

To deactivate programming mode, set ULA2 register 15 to any other value (eg 0000 binary):

OUT 36411, 240 – leaves flash programming mode

To actually program the flash chip, you must send it specific instructions (first to select a block, then to unlock it, then to erase it if necessary, THEN you can write to it, then you lock it again…). These instructions differ depending on the specific flash ROM chip.

(ULA2’s 4 bit registers are discussed in greater detail in other Prism documentation)